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RESEARCH ARTICLE

DESIGN OF LOW POWER / HIGH SPEED MULTIPLIER USING SPURIOUS POWER SUPPRESSION TECHNIQUE (SPST)

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Abstract — This project provides the experience of applying an advanced version of Spurious Power Suppression Technique (SPST) on multipliers for high speed and low power purposes. When a portion of data does not affect the final computing results, the data controlling circuits of SPST latch this portion to avoid useless data transition occurring inside the arithmetic units, so that the useless spurious signals of arithmetic units are filter out. Modified Booth Algorithm is used in this project for multiplication which reduces the number of partial product to n/2. To filter out the useless switching power, there are two approaches, i.e using registers and using AND gates, to assert the data signals of multipliers after data transition. The simulation result shows that the SPST implementation with AND gates owns an extremely high flexibility on adjusting the data asserting time which not only facilitates the robustness of SPST but also leads to a speed improvement and power reduction

Index Terms—SPST; Low Power Design; Modified Booth; FPGA; Verilog HDL

I INTRODUCTION

Multiplication is an important part of real-time digital signal processing (DSP) applications ranging from digital filtering to image processing. Lowering down the power consumption and enhancing the processing performance of the circuit designs are undoubtedly the two important design challenges of wireless multimedia and DSP applications, in which multiplications are frequently used for key computations, such as FFT, DCT, quantization, and filtering. All multiplication methods share the same basic procedure - addition of a number of partial products. A number of different methods can be used to add the partial products. The simple methods are easy to implement, but the more complex methods are needed to obtain the fastest possible speed. The simplest method of adding a series of partial products is shown in Figure 1.1. It is based upon an adder-accumulator, along with a partial product generator and a hard wired shifter. This is relatively slow, because adding N partial products requires N clock cycles. The easiest clocking scheme is to make use of the system clock, if the multiplier is embedded in a larger system. The system clock is normally much slower than the maximum speed at

which the simple iterative multiplier can be clocked, so if the delay is to be minimized an expensive and tricky clock multiplier is needed, or the hardware must be self-clocking.

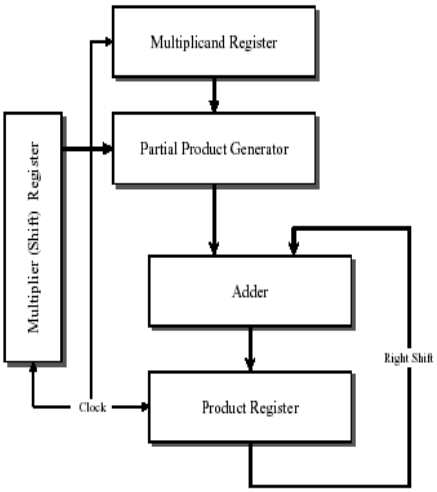

Fig 1

In this paper Modified Booth Algorithm is used with detection logic, which will suppress the needless power in the circuit and also speed has been increased. Booth Algorithm also reduces the hardware size of the circuit by reducing the partial product by half..

II SPST AS PRECOMPUTATION LOGIC

Pre Computation logic is one of the efficient Low power VLSI technique to reduce the useless power dissipation in the circuits. The influence of the spurious signal transitions illustrated as five cases of a 16-bit addition are explored as shown in Fig. 2. The case1 illustrates a transient state in which the Spurious transitions of carry signals occur in the MSP though the fina1 result of the MSP are unchanged. The 2nd and 3rd cases describe the situations of one negative operand adding another positive operand without and with carry from LSP, respectively. Moreover, the 4th 5th cases respectively demonstrate the conditions of two negative operands addition without and with carry-in from LSP. In those cases, the results of the MSP are predictable, therefore the computations in the MSP are useless and can be neglected. Eliminating those spurious computations will not only save the power consumed inside the SPST adder/subtractor but also decrease the glitching noises which will affect the next arithmetic circuits.

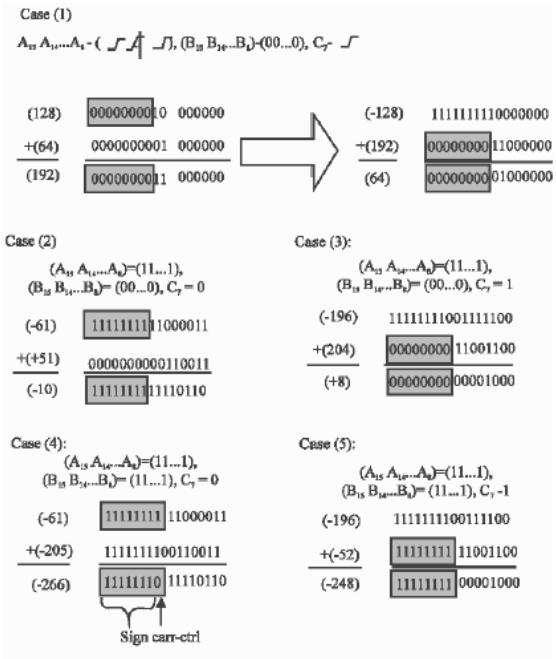

Fig 2

From the above fives cases we can design the pre computation logic circuit (Detection Logic) as shown in Figure 3 which will avoid the useless computations so that the useless power has been reduced

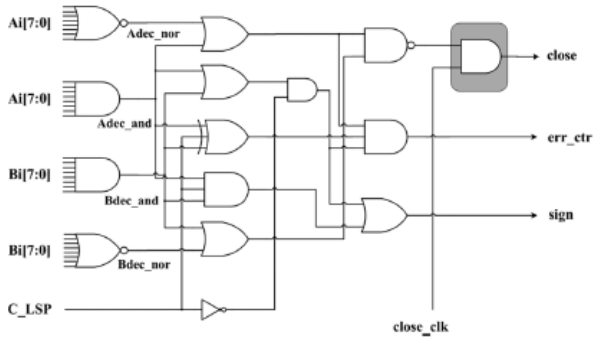

Fig 3

In this paper the above detection logic is used to detect the unwanted MSB calculations, so that unwanted power dissipations were avoided. The SPST adder can be designed by using this detection logic to achieve power efficiency while adding Partial products, such a SPST adder is shown in figure 4 below.

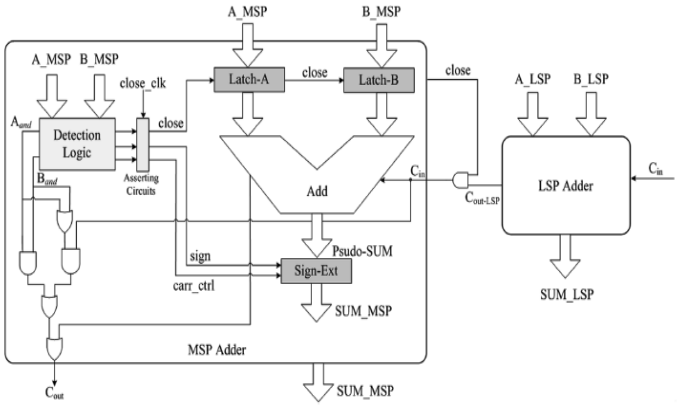

Fig 4

III LOW POWER MULTIPLIER DESIGN USING SPST

The Modified Booth algorithm is used for Multiplication with SPST technique in this paper.

A. Applying SPST on Modified Booth Encoder

While multiplying two 16 bit numbers through booth algorithm eight partial products produced, but some of the partial product may contain all the bits as zero, so saving those computations can significantly reduce the power consumption caused by the transient signals. We propose the SPST-equipped modified-Booth encoder, which is controlled by a detection unit. The detection unit has one of the two operands as its input to decide whether the Booth encoder calculates redundant computations. As shown in Fig. 5, the latches can, respectively, freeze the inputs of MUX-4 to MUX-7 or only those of MUX-6 to MUX-7 when the PP4 to PP7 or the PP6 to PP7 are zero, to reduce the transition power dissipation. Such cases occur frequently in e.g., FFT/IFFT, DCT/IDCT, and Q/IQ which are adopted in encoding or decoding multimedia data.

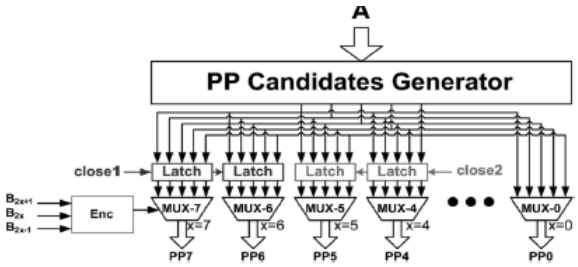

Fig 5

B. Applying SPST on Compression Tree

The proposed SPST-equipped multiplier is illustrated in Fig. 6. The PP generator generates five candidates of the partial products, i.e., {-2A; -A; 0; A; 2A}, which are then selected according to the Booth encoding results of the operand B. Moreover, when the operand besides the Booth encoded one has a small absolute value, there are opportunities to reduce the spurious power dissipated in the compression tree. According to the redundancy analysis of the additions, we replace some of the adders in compression tree of the multiplier with the SPST-equipped adders, which are marked with oblique lines in Fig. 6. The bit-widths of the MSP and LSP of each SPST-equipped adder are also indicated in fraction values nearing the corresponding adder in Fig. 6.

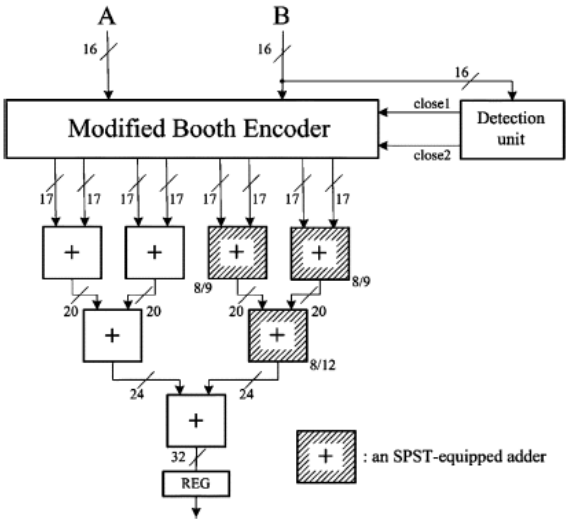

Fig 6

IV IMPLEMENTATION AND PERFORMANCE EVALUATION

The SPST equipped Multiplier is designed by writing VERILOG HDL code and simulated and synthesized using XILINX 9.1.

TABLE 1
Device Utilization for Modified Booth with SPST

Number of Slices:	231 out of 4656 4%
Number of 4 input LUTs:	430 out of 9312 3%
Number of IOs	68
Number of bonded IOBs:	68 out of 92 73%

The Maximum Combinational Path delay for Modified Booth with SPST as per this paper design is 20.1 ns. Out of this 22 n seconds 13 n seconds taken for logic and remaining for routing.

TABLE 2

Device Utilization for Ordinary Booth with SPST

Number of Slices:	254 out of 4656 5%
Number of 4 input LUTs:	483 out of 9312 5%
Number of IOs:	68
Number of bonded IOBs:	68 out of 92 73%

The Maximum Combinational Path delay for Modified Booth with SPST as per this paper design is 23.7 ns. Out of this 22 n seconds 15.5 n seconds taken for logic and remaining for routing.

V CONCLUSION

The high speed low power multiplier adopting the new SPST is designed. The Multiplier is designed by equipping SPST on a modified Booth encoder which is controlled by a detection unit using AND gate. The modified Booth encoder will reduce the number of partial products generated by a factor two. The SPST adder will avoid the unwanted addition and thus minimize the switching power dissipation. The SPST implementation with AND gate have an extremely high flexibility on adjusting the data asserting time. This facilitates the robustness of SPST can attain significant speed improvement and power reduction when compared with the conventional tree multipliers. This design verified using Xilinx 9.1 using Verilog HDL coding and successfully synthesized.

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